VL1772-02

FLOPPY DISK CONTROLLER/FORMATTER

FEATURES

- Built-in data separator
- Built-in write precompensation
- Single and double density
- Motor control
- 128, 256, 512, or 1024 sector lengths
- TTL compatible
- 8-bit bidirectional data bus
- Fast step rates
- 28-pin DIP
- Single 5 V power supply

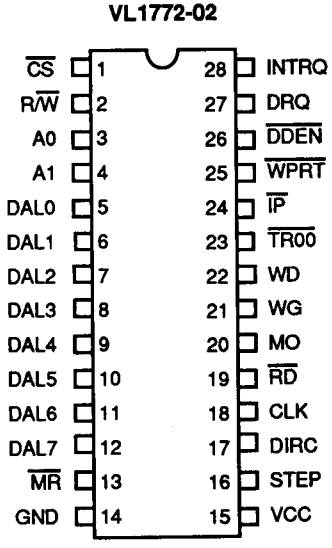
DESCRIPTION

The VL1772-02 is an MOS/LSI device that performs the functions of a floppy disk controller/formatter. It replaces the older 1770-type device. The drive side of the interface needs no additional logic except for buffers/receivers. Designed for single- or double-density operation, the device contains a programmable Motor On signal.

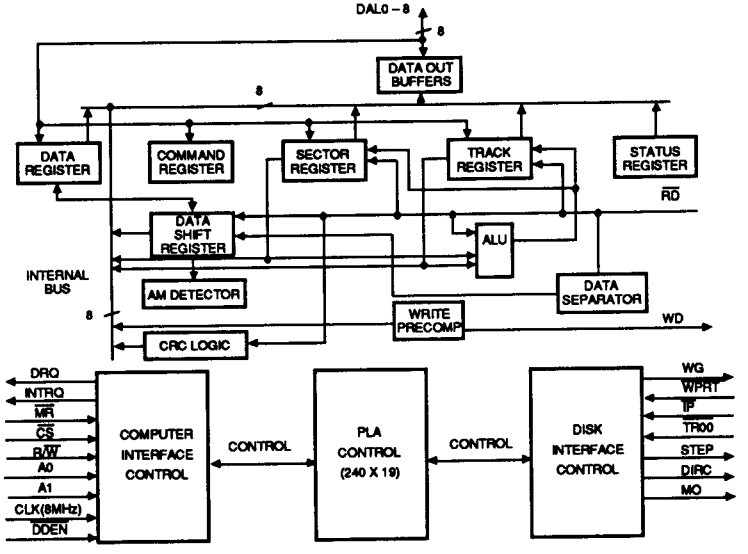
The VL1772-02 is implemented in NMOS silicon-gate technology and is available in a 28-pin dual in-line package. It is a low-cost version of the WD179X Floppy Disk Controller/ Formatter and is compatible with generic 179X types. It also has a built-in digital data separator and write precompensation circuits. A single read (RD) line (pin 19) is the only input required to recover serial FM or MFM data from the disk drive. The device has been specifically designed for control of floppy disk drives with data rates of 125K bps (single density) and 250K bps (double density). In addition, it can write a precompensation that is125 ns from nominal, and can be enabled at any point through simple software commands. Another programmable feature, Motor On, has been incorporated to automatically enable the spindle motor prior to operating a selected drive. The VL1772-02 offers stepping rates of 2, 3, 6, and 12 ms.

The processor interface consists of an 8-bit bidirectional bus for transfer of the status information, data, and commands. All host communication with the drive occurs through these data lines. They are capable of driving one standard TTL load or three LS loads.

PIN DIAGRAM



BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL1772-02PC	Plastic DIP
VL1772-02QC	Plastic Leaded Chip Carrier (PLCC)
VL1772-02CC	Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
$\overline{CS}$	1	Chip Select - A logic low on this input selects the chip and enables host communication with the device.
R/$\overline{W}$	2	Read/Write - A logic high on this input controls the placement of data on the $\overline{D0}$-$\overline{D7}$ lines from a selected register, while a logic low causes a write operation to a selected register.
A0, A1	3, 4	Address 0, 1 - These two inputs select a register to read or write data:

$\overline{CS}$	A1	A0	R/$\overline{W}$ = 1	R/$\overline{W}$ = 0
0	0	0	Status Register	Command Register
0	0	1	Track Register	Track Register
0	1	0	Sector Register	Sector Register
0	1	1	Data Register	Data Register

DAL0 - DAL7	5 - 12	Data Access Lines 0 through 7 - Eight-bit bidirectional bus used for transfer of data, control, or status. This bus is enabled by $\overline{CS}$ and R/$\overline{W}$. Each line drives one TTL load.
$\overline{MR}$	13	Master Reset - A logic low pulse on this line resets the device and initializes the status register (internal pull-up).
GND	14	Ground - Ground
VCC	15	Power Supply - +5 V ±5% power supply input.
STEP	16	Step - The Step output contains a pulse for each step of the drive's R/$\overline{W}$ head. This is a pulse to the disk drive.
DIRC	17	Direction - The Direction output is high when stepping in towards the center of the diskette, and low when stepping out.
CLK	18	Clock - This input requires a free-running 50% duty cycle clock (for internal timing) at 8 MHz ±1%.
$\overline{RD}$	19	Read Data - This active-low input is the raw data line containing both clock and data pulses from the drive.
MO	20	Motor On - Active high output used to enable the spindle motor prior to read, write, or stepping operations.
WG	21	Write Gate - This output is made valid prior to writing on the diskette.
WD	22	Write Data - FM or MFM clock and data pulses are placed on this line to be written on the diskette.
$\overline{TR00}$	23	Track 00 - This active-low input informs the VL1772-02 that the drive's R/$\overline{W}$ heads are positioned over Track zero (internal pull-up).
$\overline{IP}$	24	Index Pulse - This active-low input informs the VL1772-02 when the physical index hole has been encountered on the diskette (internal pull-up).
$\overline{WPRT}$	25	Write Protect - This input is sampled whenever a Write Command is received. A logic low on this line prevents any Write Command from executing (internal pull-up).
$\overline{DDEN}$	26	Double Density Enable - This input pin selects either single (FM) or double (MFM) density. When $\overline{DDEN}$ = 0, double density is selected (internal pull-up).
DRQ	27	Data Request - This active-high output indicates that the Data Register is full (on a Read) or empty (on a Write) operation.
INTRQ	28	Interrupt Request - This active-high output is set at the completion of any command or a read of the Status Register.

ARCHITECTURE

TheVL1772-02 Floppy Disk Controller/ Formatter block diagram is illustrated on the front page. The primary sections include the parallel processor interface and the floppy disk interface.

Data Shift Register - This 8-bit register assembles serial data from the Read Data input ($\overline{RD}$) during read operations and transfers serial data to the Write Data output during write operations.

Data Register - This 8-bit register is used as a holding register during disk read and write operations. In disk read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In disk write operations, information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command, the Data Register holds the address of the desired track position. This register is loaded from the Data Access Lines (DAL) and gated onto the DAL under processor control.

Track Register - This 8-bit register holds the track number of the current read/ write head position. It is incremented by one every time the head is stepped in and decremented by one every time the head is stepped out (towards Track 00). The contents of the register are compared with the recorded track number in the ID field during disk read, write, and verify operations. The Track Register can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Sector Register (SR) - This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk read or write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) - This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy, unless the new command is a forced interrupt. The Command Register can be loaded from the DAL but not read onto the DAL.

Status Register (STR) - This 8-bit register holds device status information. The meaning of the status bits is a function of the type of command previously executed. This register can be read onto the DAL but not loaded from the DAL.

CRC Logic - This logic is used to check or to generate the 16-bit cyclic redundancy check (CRC). The polynomial is:

$$G(x) = x^{16} + x^{12} + x^5 + 1$$

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

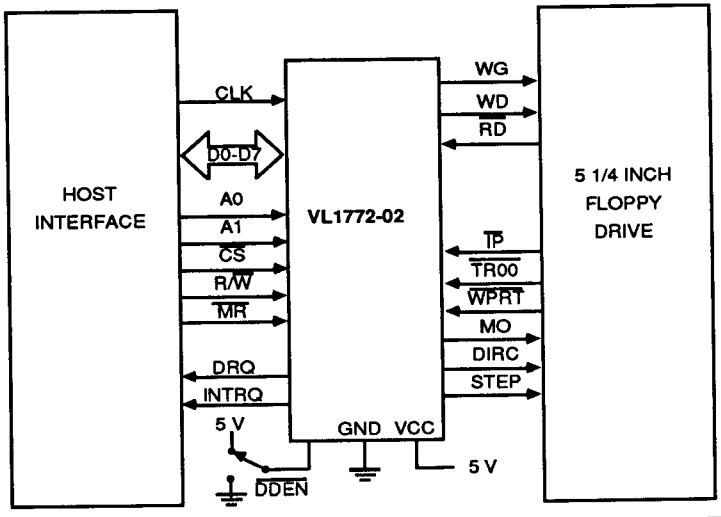
Arithmetic/Logic Unit (ALU) - The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk-recorded ID field.

Timing and Control - All computer and floppy disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock. The VL1772-02 has two different modes of operation according to the state of $\overline{DDEN}$: When $\overline{DDEN}$ = 0, double density (MFM) is enabled. When $\overline{DDEN}$ = 1, single density is enabled.

Address Mark Detector - The AM detector detects ID, data, and index address marks during read and write operations.

Data Separator - A digital data separator, consisting of a ring shift register and data window detection logic, provides read data and a recovery clock to the AM detector.

FIGURE 1. SYSTEM BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight data access lines (DALs) and associated control signals. The DALs are used to transfer data, status, and control words out of, or into the VL1772-02. The DALs are three-state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) = 0 and R/$\overline{W}$ = 1 are active, or act as input receivers when $\overline{CS}$ and R/$\overline{W}$ = 0 are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signal R/$\overline{W}$ during a read or write operation, are interpreted as selecting the following registers:

A1	A0	READ (R/$\overline{W}$ = 1)	WRITE (R/$\overline{W}$ = 0)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

After any register is written to, the same register cannot be read from until 16 µs in MFM or 32 µs in FM have elapsed.

During direct memory access (DMA) types of data transfers between the Data Register of the VL1772-02 and the processor, the Data Request (DRQ) output is used in data transfer control. This signal also appears as status bit 1 during read and write operations.

On disk read operations, the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The read operation continues until the end of sector is reached.

On disk write operations, the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the floppy disk, a byte of zeros is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated; it is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The VL1772-02 has two modes of operation, according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input is at 8 MHz.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512, or 1024 bytes are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1". For MFM formats, $\overline{DDEN}$ should be placed to a logical "0".

Sector lengths are determined at format time by the fourth byte in the "ID" field.

SECTOR LENGTH TABLE

SECTOR LENGTH FIELD (HEX)	NUMBER OF BYTES IN SECTOR (DECIMAL)
00	128
01	256
02	512
03	1024

There are from 0 to 244 sectors per track for the VL1772-02, and from 0 to 244 tracks.

GENERAL DISK WRITE OPERATION

When writing is to take place on the disk the Write Gate (WG) output is activated, allowing current to flow into the read/write head. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register in response to a Data Request from the device before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated, and the Write Protect status bit is set.

For write operations, the VL1772-02 provides Write Gate to enable a write condition, and Write Data which consists of a series of active-high pulses. These pulses contain both clock and data information in FM and MFM. Write Data provides the unique missing clock patterns for recording address marks.

The Precompensation Enable bit in Write commands allow automatic write precompensation to take place. The outgoing write data stream is delayed or advanced from nominal by 187ns according to the following table:

PATTERN				MFM	FM
X	1	1	0	Early	N/A
X	0	1	1	Late	N/A
0	0	0	1	Early	N/A
1	0	0	0	Late	N/A

Next Bit to be sent
Current Bit sending
Previous Bits sent

Precompensation is typically enabled on the innermost tracks where bit shifts usually occur and bit density is at its maximum.

COMMANDS

The VL1772-02 accepts eleven commands. Command words should only be loaded in the Command Register when the Busy Status Bit is off (Status Bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy Status Bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault-free. For ease of discussion, commands are divided into four types and are summarized in Table 1.

The Type I Commands (see Figure 2) include the Restore, Seek, Step, Step-in, and Step-out commands. Each of the Type I Commands contains a rate field (r0, r1), which determines the stepping motor rate.

A 4 µs (MFM) or 8 µs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active-high when stepping in and low when stepping out. The Direction signal is valid 24 µs before the first stepping pulse is generated.

After the last directional step, an additional 30 ms of head settling time takes place if the Verify flag is set in Type I commands. There is also a 30 ms head settling time if the E flag is set in any Type II or III command.
When a Seek, Step, or Restore command is executed, an optional verification of read/write head position can be performed by setting bit 2 (V = 1) in the command word to logic 1. The verification operation begins at the end of the 30 ms settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field cyclic redundancy check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC Error Status Bit is set (Status Bit 3), and the next encountered ID field is read from the disk for the verification operation.

The VL1772-02 must find an ID field with correct track number and correct CRC within five revolutions of the media, otherwise, the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

All commands, except the Force Interrupt command, may be programmed via the h Flag to delay for spindle motor start up time. If the h Flag is not set and the Motor On line is low when a command is received, the VL1772-02 will force Motor On to a logic 1 and waits six revolutions before executing the command. At 300 RPM, this guarantees a one-second spindle start-up time. If, after finishing the

TABLE 1. COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step-in	0	1	0	u	h	V	r_1	r_0
I	Step-out	0	1	1	u	h	V	r	r_0
II	Read Sector	1	0	0	m	h	E	0	0
II	Write Sector	1	0	1	m	h	E	P	a_0
III	Read Address	1	1	0	0	h	E	0	0
III	Read Track	1	1	1	0	h	E	0	0
III	Write Track	1	1	1	1	h	E	P	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

FLAG SUMMARY

TYPE I COMMANDS

h = Motor On Flag (Bit 3)

h = 0, Enable Spin-up Sequence
h = 1, Disable Spin-up Sequence

V = Verify Flag (Bit 2)

V = 0, No Verify
V = 1, Verify on Destination Track

r_1, r_0 = Stepping Rate (Bits 1,0)

r_1	r_0	1772-02
0	0	6 ms
0	1	12 ms
1	0	2 ms
1	1	3 ms

u = Update Flag (Bit 4)

u = 0, No Update
u = 1, Update Track Register

TYPE II & III COMMANDS

m = Multiple Sector Flag (Bit 4)

m = 0, Single Sector
m = 1, Multiple Sector

H = Motor On Flag (Bit 3)

H = 0, Enable Spin Up Sequence
H = 1, Disable Spin Up Sequence

a_0 = Data Address Mark (Bit 0)

a_0 = Write Normal Data Mark
a_0 = 1, Write Deleted Data Mark

E = 15ms Settling Delay (Bit 2)

E = 0, No Delay
E = 1, Add 15ms Delay

P = Write Precompensation (Bit 1)

P = 0,Enable Write Precomp
P = 1,Disable Write Precomp

TYPE IV COMMANDS

I_3-I_0 Interrupt Condition (Bits 3-0)

I_0 = 1, Not Used
I_1 = 1, Not Used
I_2 = 1, Interrupt on Index Pulse
I_3 = 1, Immediate Interrupt
I_3-I_0 = 0, Terminate without interrupt

command, the device remains idle for ten revolutions, the Motor On line goes back to a logic 0. If a command is issued while Motor On is high, the command executes immediately, defeating the six-revolution start up. This feature allows consecutive read or write commands without waiting for each motor start-up; the VL1772-02 assumes the spindle motor is up to speed.

RESTORE (SEEK TRACK 0)

Upon receipt of this command, the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active-low indicating the read/write head is positioned over Track 00, the Track Register is loaded with zeros and an interrupt is generated. If $\overline{TR00}$ is not active-low, stepping pulses (pin 16) at a rate specified by the r1, r0 field are issued until the $\overline{TR00}$ input is activated. At this time, the Track Register is loaded with zeros and an interrupt is generated. If the $\overline{TR00}$ input does not go active-low after 255 stepping pulses, the VL1772-02 terminates operation, interrupts, and sets the Seek Error Status Bit, providing the V flag is set. A verification operation also takes place if the V flag is set. The h bit allows the Motor On option at the start of command.

FIGURE 2. TYPE I COMMAND FLOWCHART

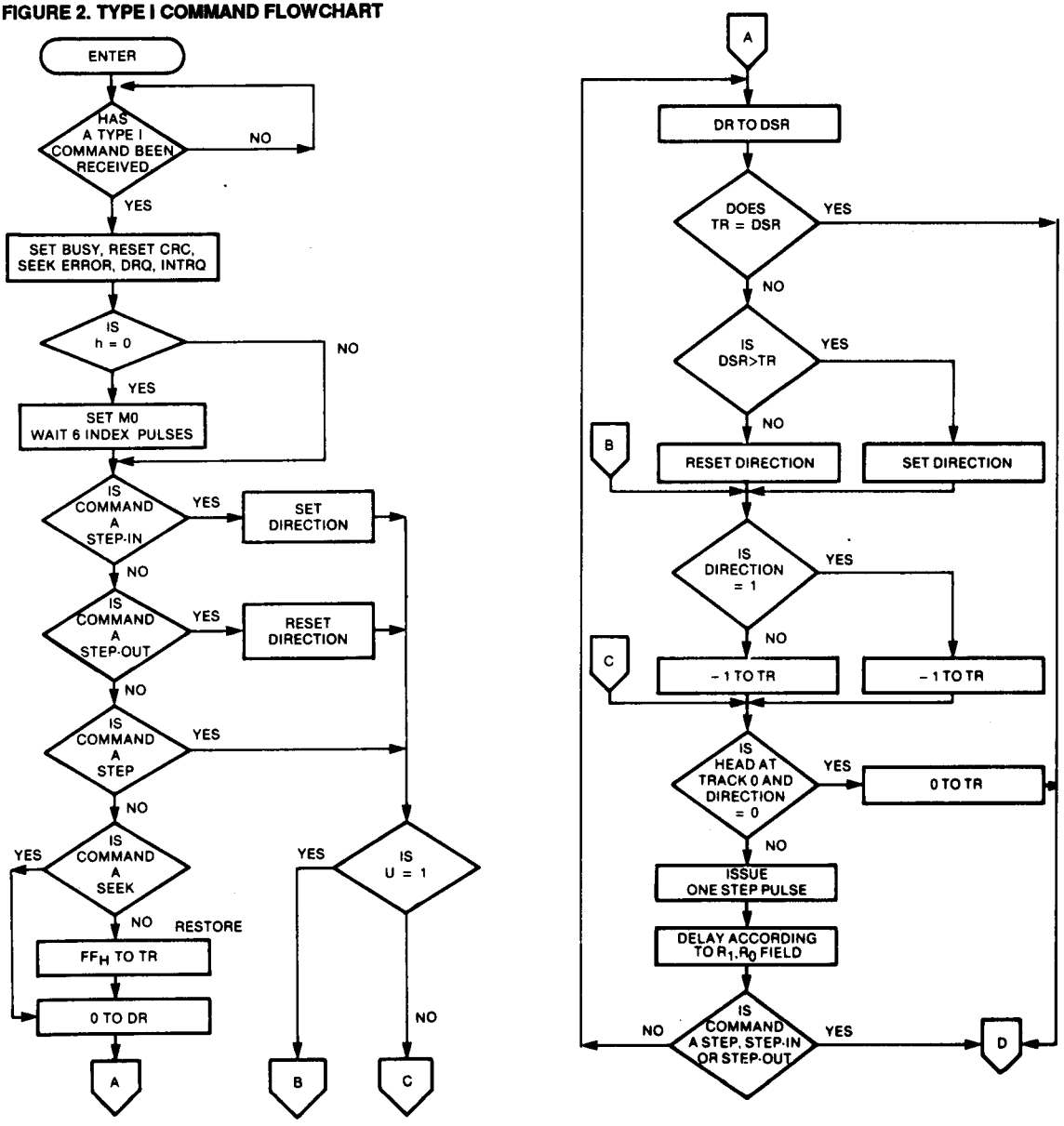


FIGURE 2. TYPE I COMMAND FLOWCHART (Cont.)

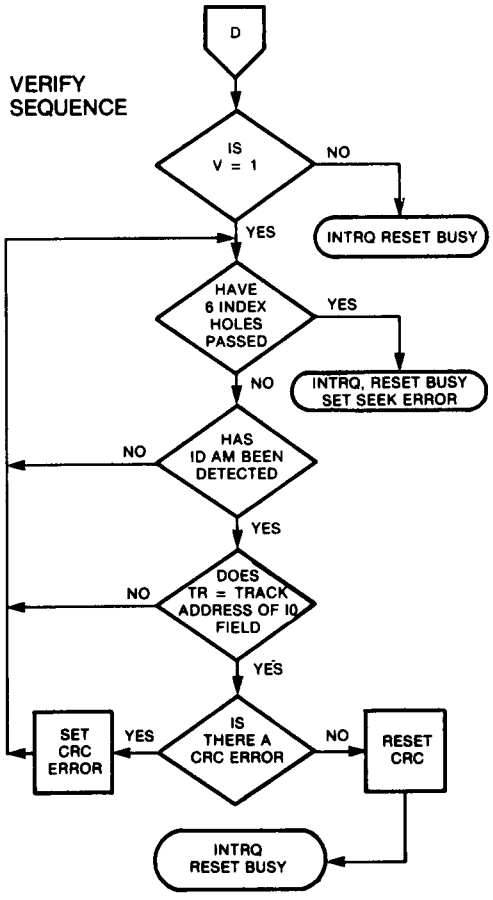
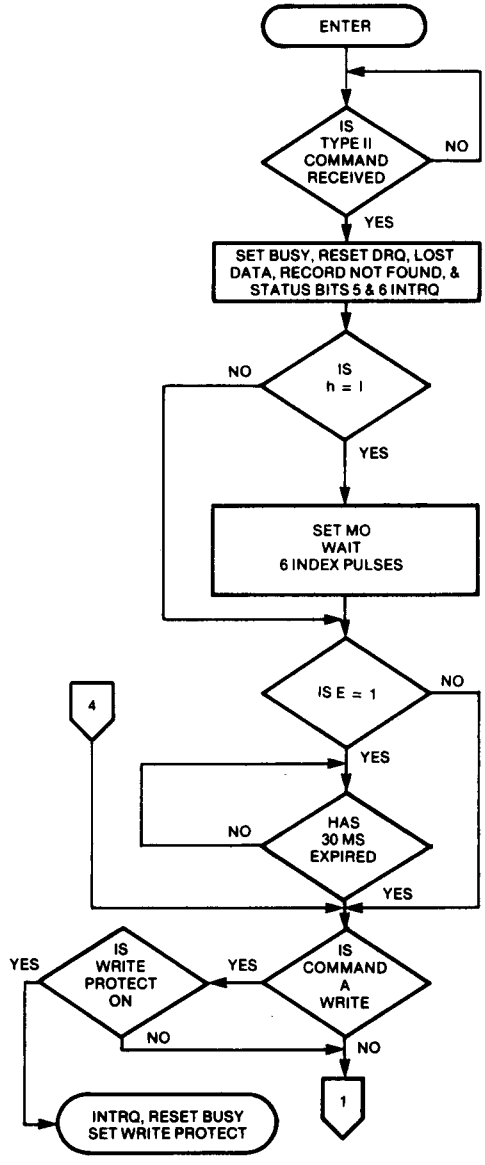


FIGURE 3. TYPE II COMMAND FLOWCHART



SEEK
This command assumes that the Track Register contains the track number of the current position of the read/write head and the Data Register contains the desired track number. The VL1772-02 will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command. (Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.)

STEP
Upon receipt of this command, the VL1772-02 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1, r0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN
Upon receipt of this command, the VL1772-02 issues one stepping pulse in the direction towards track 76. If the U flag is on, the Track Register is incremented by one. After a delay is determined by the r1, r0 field, a verification takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT
Upon receipt of this command, the VL1772-02 issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After a delay determined by the r1, r0 field, a verification takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS
The Type II Commands (see Figure 3) are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status bit is set. If the E flag = 1, the command executes after a 15 ms delay.

When an ID field is located on the disk, the VL1772-02 compares the track number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the sector number of the ID field is compared with the Sector Register. If there is not a sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and is either written into or read from depending upon the command. The VL1772-02 must find an ID field with a track number, sector number, and CRC within four revolutions of the disk; otherwise, the Record Not Found Status Bit is set (Status Bit 4) and the command is terminated with an interrupt (INTRQ).

Each of the Type II Commands contains an m flag that determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The VL1772-02 continues to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: if the VL1772-02 is instructed to read sector 27 and there are only 26 sectors on the track, the sector register exceeds the number available. The VL1772-02 will search for five disk revolutions, interrupt out, reset busy, and set the Record Not Found Status Bit.

READ SECTOR
Upon receipt of the Read Sector command, the Busy status bit is set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The data address mark (DAM) of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field is searched for and verified again followed by the data address mark search. If, after five revolutions the DAM cannot be found, the Record Not Found StatusBit is set and the operation is terminated. When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred, that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been input to the computer. If there is a CRC error at the end of the data field, the CRC Error Status Bit is set, and the command is terminated (even if it is a multiple record command).
At the end of the read operation, the type of data address mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR
Upon receipt of the Write Sector command, the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The VL1772-02 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time, the data

FIGURE 3. TYPE II COMMAND FLOWCHART (Cont.)

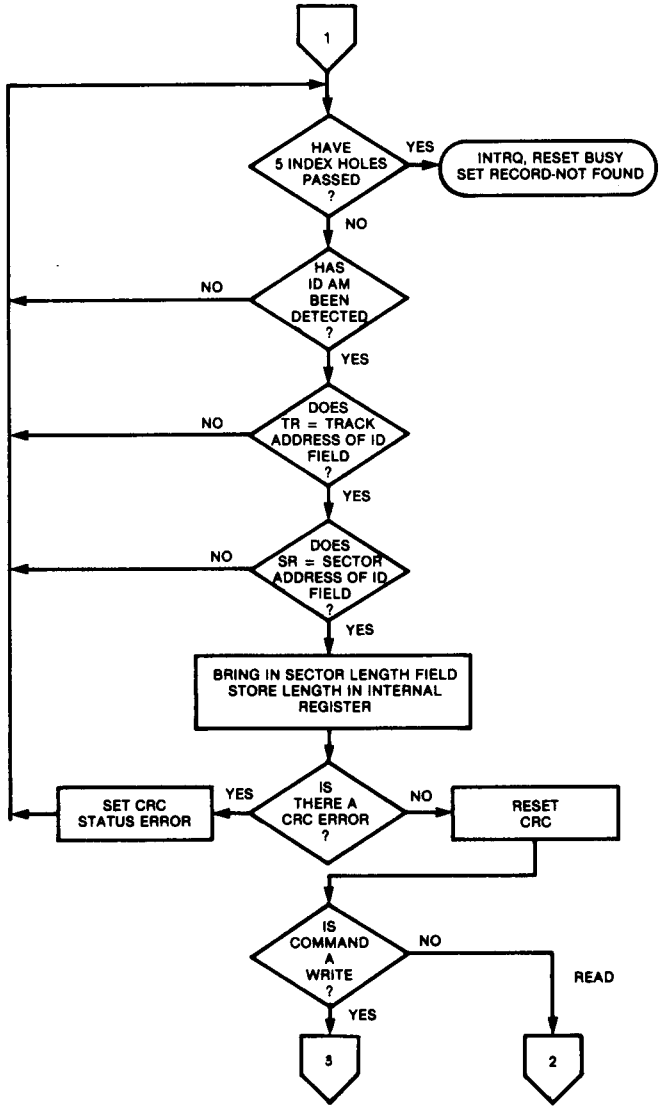


FIGURE 3. TYPE II COMMAND FLOWCHART (Cont.)

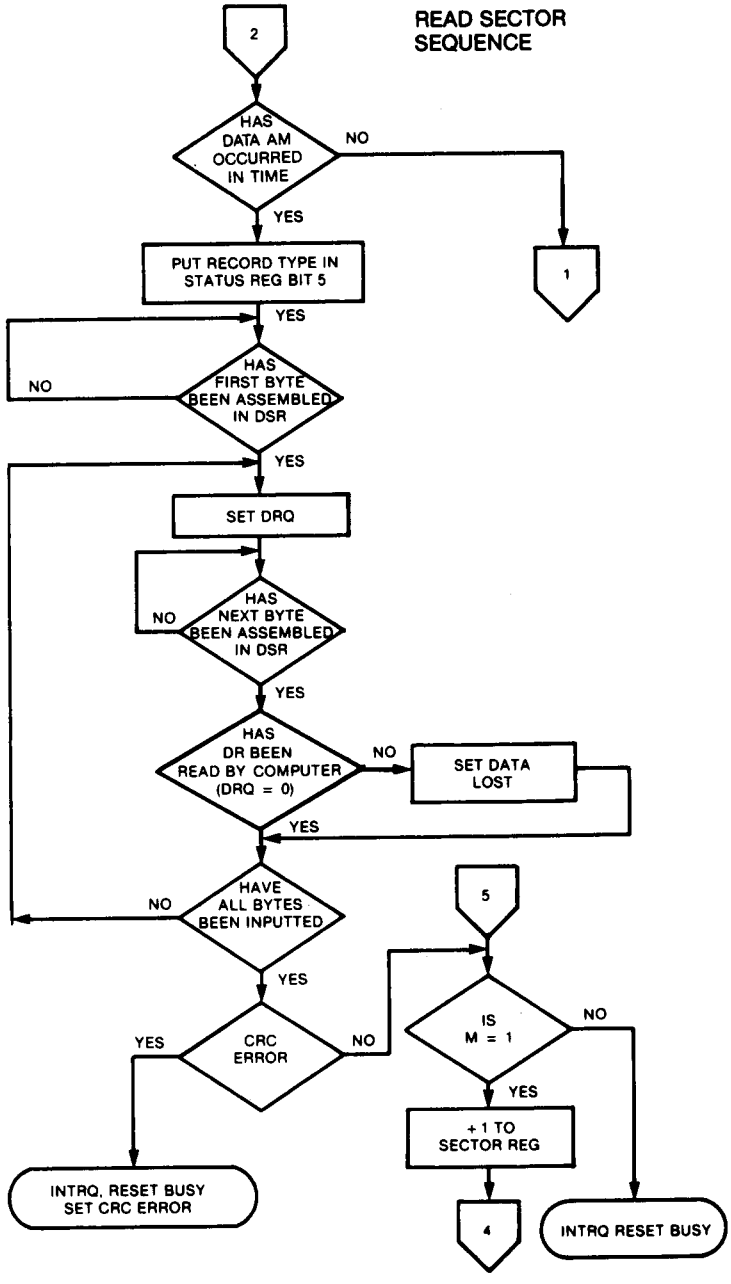
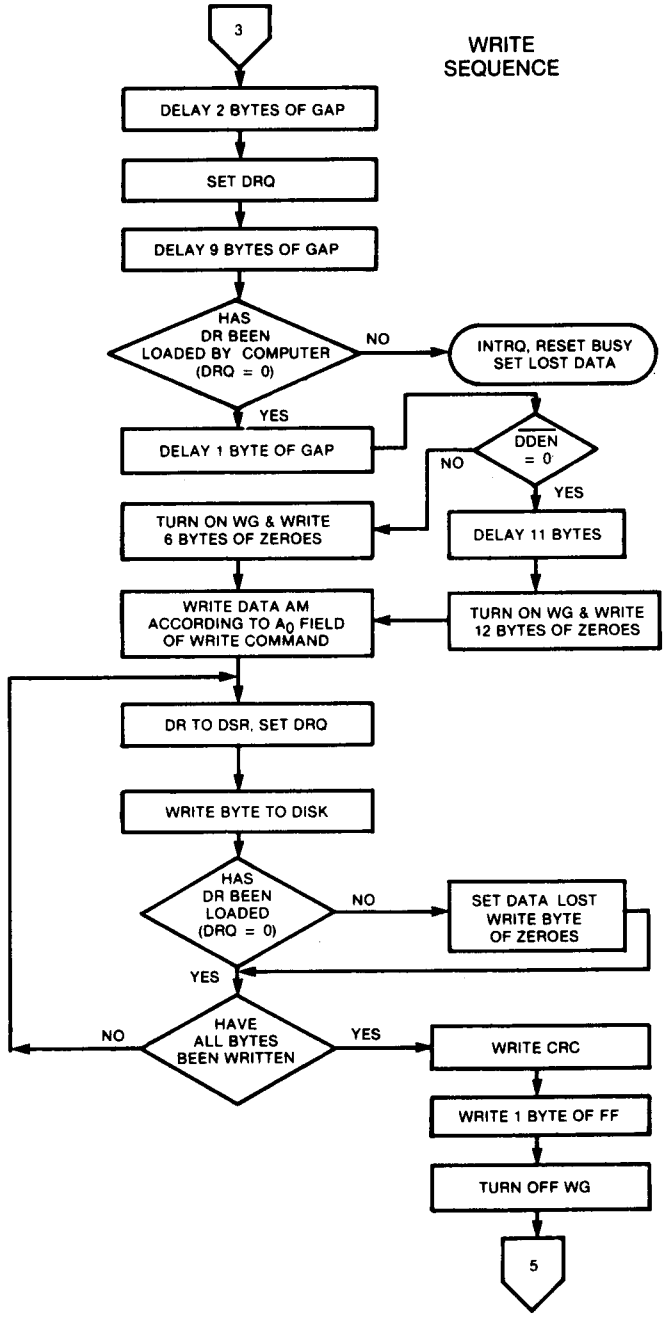


FIGURE 3. TYPE II COMMAND FLOWCHART (Cont.)



address mark is then written on the disk as determined by the a0 field of the command as shown below:

a_0	DATA ADDRESS MARK (BIT 0)
1	Deleted Data Mark
0	Data Mark

The VL1772-02 then writes the data field and generates DRQs to the computer. If the DRQ is not serviced in time for continuous writing, the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in FMF. The WG output is then deactivated. INTRQ will set 24 µs (MFM) after the last CRC byte is written. For partial sector writing, the proper method is to write data and fill the balance with zeros.

TYPE III COMMANDS

Read Address - Upon receipt of the Read Address command, the Busy Status Bit is set. The next-encountered ID field is then read in from the disk, and six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDR	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the VL1772-02 checks for validity and the CRC Error Status Bit is set if there is a CRC error. The track address of the ID field is written into the Sector Register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy status is reset.

Read Track - Upon receipt of the READ track command, the head is loaded and the Busy status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All gap, header, and data bytes are assembled and transferred to the Data Register and DRQs are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics that make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; and the address mark detector is on for the duration of the command. Because the AM detector is always on, write splices or noise may cause the chip to look for an AM.

The ID AM, ID Field, ID CRC Bytes, DAM, Data and Data CRC Bytes for each sector will be correct. The Gap Bytes
may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

Data and gap information are provided at the computer interface. Formatting the disk is accomplished by positioning the R/$\overline{W}$ head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the Busy Status Bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded within three byte times, the operation is terminated, making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted.
This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the VL1772-02 detects a data pattern of F5 through FE in the data register, this is interpreted as a data address mark with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern generates two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE must not appear in the gaps, data fields, or ID fields. Also, CRCs must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

TABLE 2. DATA PATTERN DECODE

DATA PATTERN IN DR (HEX)	IN FM ($\overline{DDEN}$ = 1)	IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Present CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F9 thru FB	Write F8 thru FB, CLK = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with CLK = D7	Write FC in MFM
FD	Write FD with CLK = FF	Write FD in MFM
FE	Write FE, CLK = C7, Preset CRC	Write FE in MFM
FF	Write FF with CLK = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5.
**Missing clock transition between bits 3 and 4.

TYPE IV COMMANDS

The Forced Interrupt Command is generally used to terminate a multiple sector read or write command or to ensure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set) the command is terminated and the Busy Status Bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

I0 = Don't Care
I1 = Don't Care
I2 = Every Index Pulse
I3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I3-I0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line goes high signifying that the condition specified has occurred. If I3-I0 are all set to zero (HEX D0), no interrupt occurs but any command presently under execution is immediately terminated. When using the immediate interrupt condition (I3 = 1) an interrupt immediately is generated and the current command terminated. Reading the Status or writing to the Command Register does not automatically clear the interrupt. The HEX D0 is the only command that enables the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.

Wait 16 µs (double density) or 32 µs (single density) before issuing a new command after issuing a forced interrupt. Loading a new command sooner than this nullifies the forced interrupt.

Force Interrupt Command stops any command at the end of an internal micro instruction and generates INTRQ when the specified condition is met. Force Interrupt waits until ALU operations in progress are complete (CRC calculations, compares, etc.).

Status Register - Upon receipt of any command, except the Force Interrupt command, the Busy Status Bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status Bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data Register is read the DRQ bit in the Status Register and the DRQ line are automatically reset. A write to the Data Register also causes both DRQ's to reset.

The Busy Bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a Busy status check is not recommended because a read of the Status Register to determine the condition of busy resets the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Because of internal synchronization cycles, certain time delays are observed when operating under program I/O as shown.

Operation	Next Operation	Delay Req'd. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	48µsec	24µsec
Write to Command Reg.	Read Status Bits 1-7	64µsec	32µsec
Write Register	Read Same Register	32µsec	16µsec

RECOMMENDED - 126 BYTES/SECTOR

Shown below is the recommended single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
10	FF (or 00)
369**	FF (or 00)

**Continue writing until VL1772-02 interrupts out. Approximately 369 bytes.

256 BYTES/SECTOR

Shown below is the recommended dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track comand and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
60	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01 (Sector Length)
1	F7 (2 CRC's written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (Data Address Mark)
24	4E
668**	4E

** Continue writing until VL1772-02 interrupts out. Approximately 668 bytes.

Non-Standard Formats - Variations in the recommended formats are possible to a limited extent, if the following requirements are met:

1) Sector size must be 126, 256, 512 or 1024 bytes.
2) Gap 2 cannot be varied from the recommend format.
3) Three bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the VL1772-02. Gap 1, 3, and 4 lengths can be as short as two bytes for VL1772-02 operation; however, PLL lock up time, motor speed variation, write-splice area, etc. add more bytes to each gap to achieve proper operation. For highest system reliability, use the recommended format.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

TABLE 3. STATUS REGISTER

BIT NAME	MEANING
S7 MOTOR ON	This bit reflects the status of the Motor On output.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/SPIN-UP	When set, this bit indicates that the Motor Spin-Up sequence has completed (5 revolutions) on Type I commands. Type 2 & 3 commands, this bit indicates record Type. 0 = Data Mark. 1 = Deleted Data Mark.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error data field. This bit is reset when updated.
S2 LOST DATA/ BYTE	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated. On Type I commands, this bit reflects the status of the TR00 signal.
S1 DATA REQUEST INDEX	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated. On Type 1 commands, this bit indicates the status of the IP signal.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

FIGURE 4. TYPE III COMMAND WRITE TRACK FLOWCHART

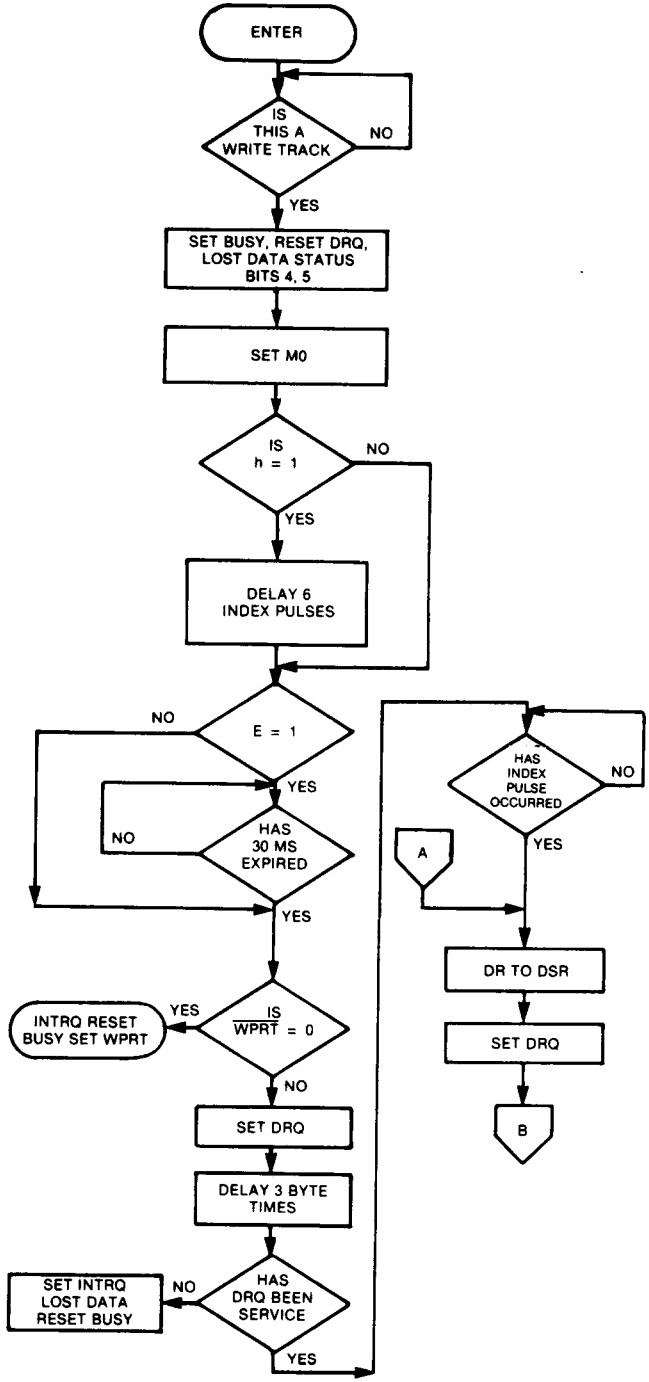


FIGURE 4. TYPE III COMMAND WRITE TRACK FLOWCHART (Cont.)

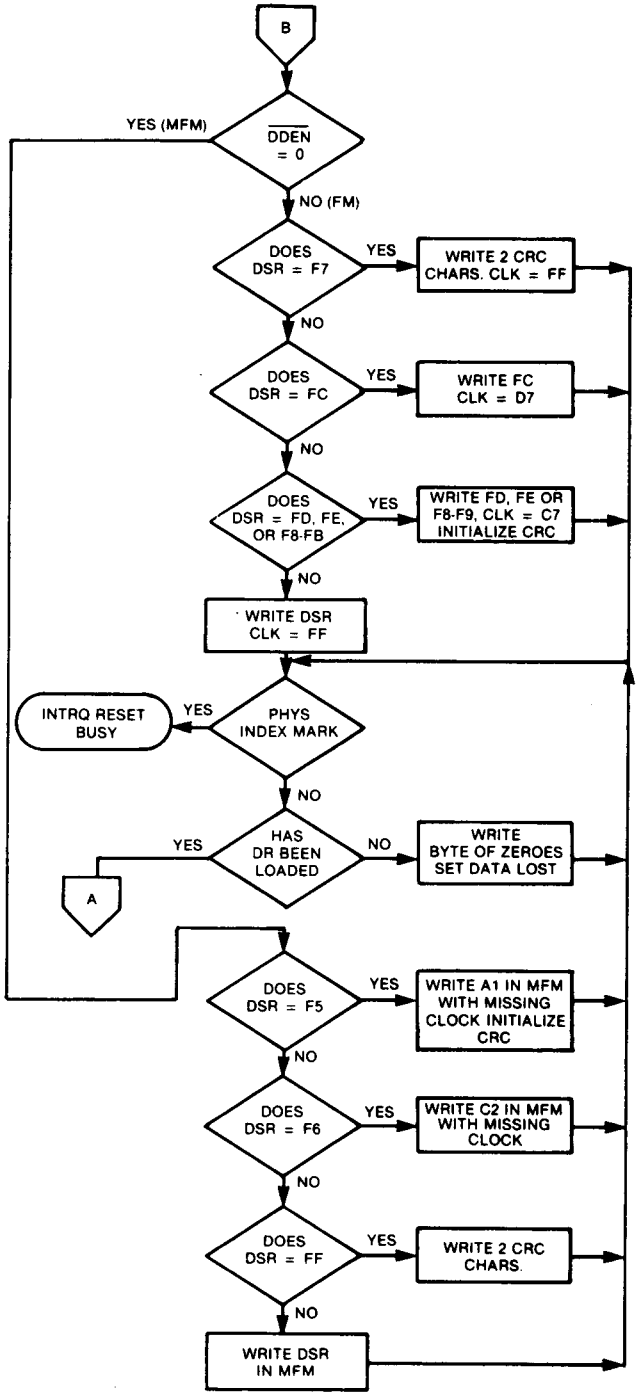


TABLE 4. READ DATA TIMING

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$\overline{\text{Raw Read}}$ Pulse Width	.200		3	μsec	MFM
	.400		3		FM
$\overline{\text{Raw Read}}$ Cycle Time	3			μsec	

TABLE 5. READ ENABLE TIMING

READ ENABLE TIMING – $\overline{RE}$ such that: R/$\overline{W}$ = 1, CS = 0.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{RE}	$\overline{RE}$ Pulse Width of $\overline{CS}$	200			nsec	C_L = 50 pf
t_{DRR}	DRQ Reset from $\overline{RE}$		200	300	nsec	
t_{DV}	Data Valid from $\overline{RE}$		100	200	nsec	C_L = 50 pf
t_{DOH}	Data Hold from $\overline{RE}$	20		150	nsec	C_L = 50pf
	INTRQ Reset from $\overline{RE}$			8	μsec	

Note: Worst case service time for DRQ is 23.5 μsec for MFM and 47.5 μsec for FM.

FIGURE 5. READ ENABLE TIMING

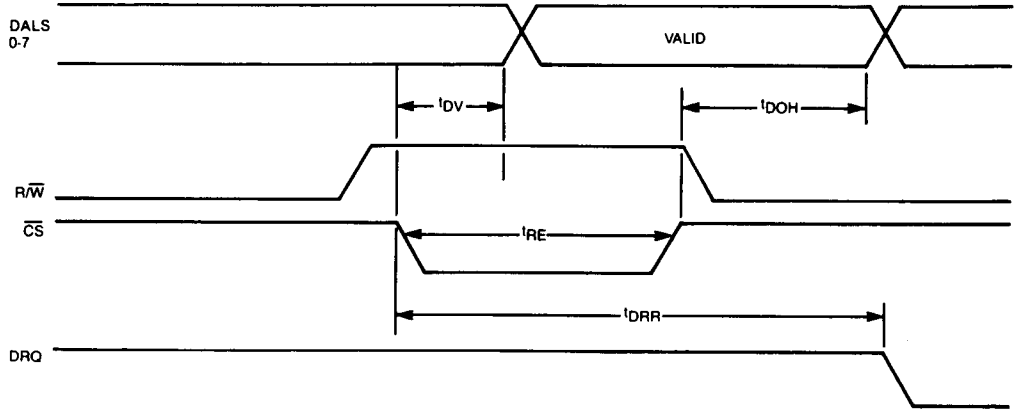


TABLE 6. WRITE ENABLE TIMING

WRITE ENABLE TIMING - $\overline{WE}$ such that: R/$\overline{W}$ = 0, $\overline{CS}$ = 0.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{AS}	Setup ADDR to $\overline{CS}$	50			nsec	
t_{SET}	Setup R/$\overline{W}$ to $\overline{CS}$	0			nsec	
t_{AH}	Hold ADDR from $\overline{CS}$	10			nsec	
t_{HLD}	Hold R/$\overline{W}$ from $\overline{CS}$	0			nsec	
t_{WE}	$\overline{WE}$ Pulse Width	200			nsec	
t_{DRW}	DRQ Reset from $\overline{WE}$		100	200	nsec	
t_{DS}	Data Setup to $\overline{WE}$	150			nsec	
t_{DH}	Data Hold from $\overline{WE}$	0			nsec	
	INTRQ Reset from $\overline{WE}$			8	μsec	

FIGURE 6. WRITE ENABLE TIMING

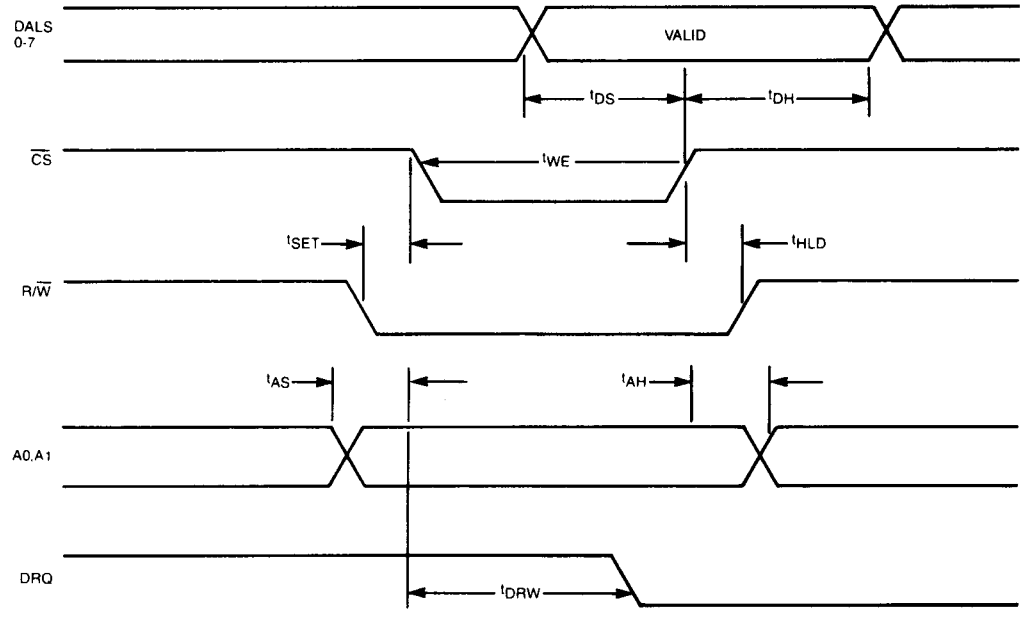


TABLE 7. WRITE DATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
	Write Gate to Write Data		4		µsec	FM
			2		µsec	MFM
	Write Data Cycle Time		4,6,8		µsec	
	Write Gate off from WD		4		µsec	FM
			2		µsec	MFM
t_{WP}	Write Data Pulse Width		820		nsec	Early MFM
			690		nsec	Nominal MFM
			570		nsec	Late MFM
			1.38		µsec	FM

FIGURE 7. WRITE DATA TIMING

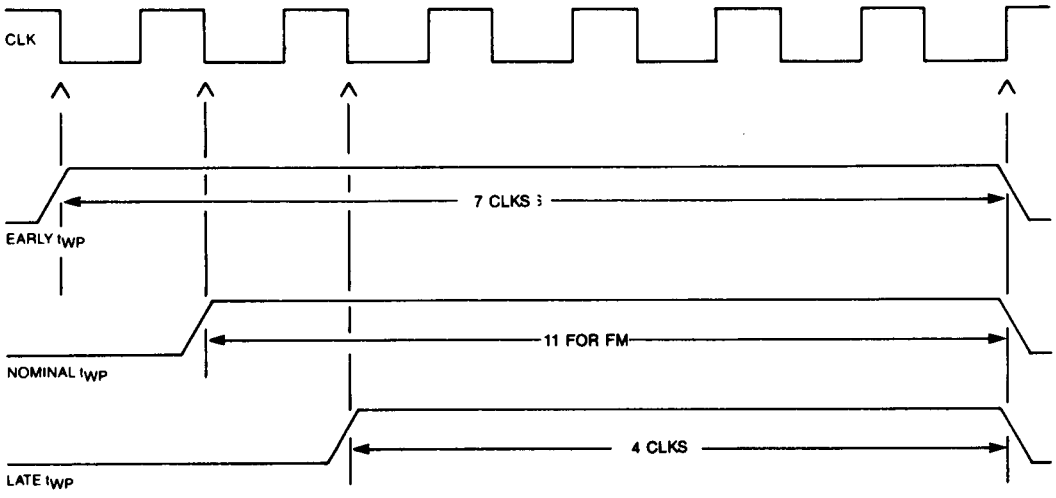


TABLE 8. MISCELLANOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{CD1}	Clock Duty (low)	50	67		nsec	
t_{CD2}	CLock Duty (high)	50	67		nsec	
t_{STP}	Step Pulse Output		4		µsec	MFM
			8			FM
t_{DIR}	Dir Setup to Step		24		µsec	MFM
			48			FM
t_{MR}	Master Reset Pulse Width	50			µsec	
t_{IP}	Index Pulse Width	20			µsec	

FIGURE 8. MISCELLANOUS TIMING

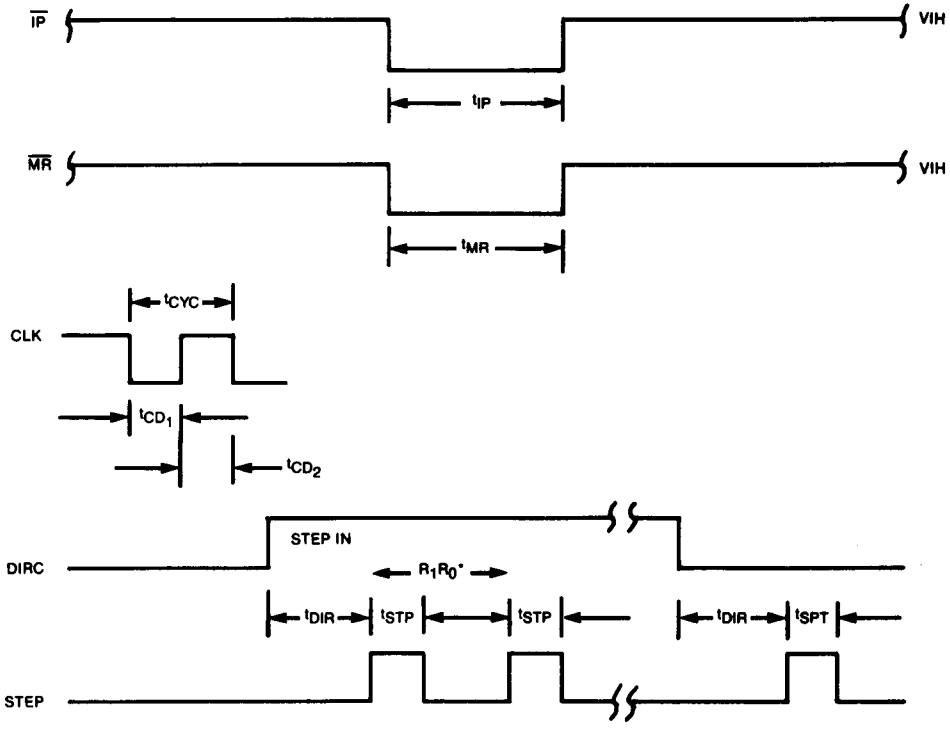
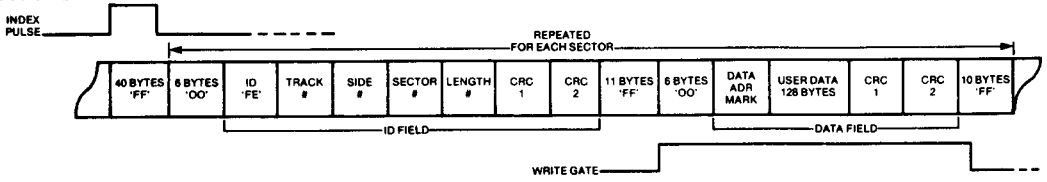
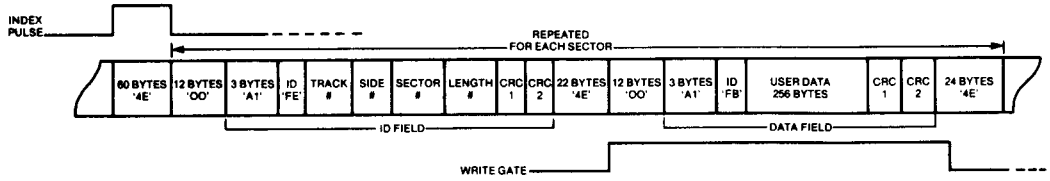


FIGURE 9. FORMATS



SINGLE DENSITY FORMAT



DOUBLE DENSITY FORMAT

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	-10°C to +80°C
Storage Temperature	-65°C to +140°C
Supply Voltage to Ground Potential	-0.5 V to +7.0 V
Applied Output Voltage	-0.5 V to +7.0 V
Applied Input Voltage	-0.5 V to +7.0 V
Power Dissipation	800 mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5 V ± 5%

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VOH	Output High Voltage	2.4			V	IO = -100 µA
VOL	Output Low Voltage			0.4	V	IO = 1.6 mA
VIH	Input High voltage	2.0			V	
VIL	Input Low Voltage			0.8	V	
IIL	Input Leakage Current			10	µA	VIN = VCC
IOL	Output Leakage Current			10	µA	VOUT = VCC
RPU	Internal Pull-up	100		1700	µA	VIN = 0 V
ICC	Operating Supply Current		75	150	mA	
PD	Power Dissipation		780		mW	

APPLICATION INFORMATION

VL1772-02: AN IMPROVED VERSION OF THE 1770-00

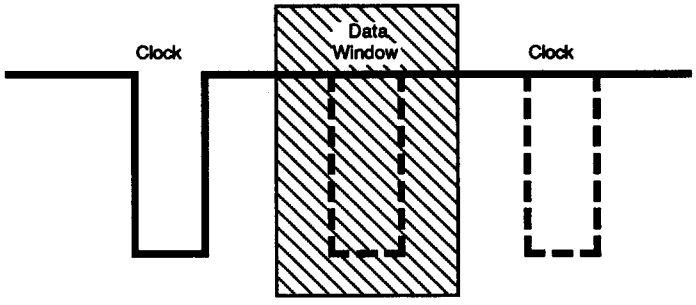
The 177X family of flexible disk controllers has attracted a great deal of interest from system designers. Allowing compactness and superior performance, this family of advanced ICs has proven to be a success in the marketplace. The original 1770-00 won much approval with its 28-pin package. Its digital data separator allowed consistent operation over temperature, but more was required. The error rate of this data recovery circuit was too high, and a reliable data separator with lower error rates was seen as an important need for computer systems of all types. In addition, a small change of step rate selections could ensure faster throughput, while maintaining compatibility with existing designs.

Thus began the design of a new concept in flexible disk controllers. An important need was to maintain compatibility with existing designs using the 1770-00, while extending the capabilities of the 177X family to include higher-performance drives. These criteria have been satisfied with the VL1772-02.

IMPROVING THE DATA SEPARATOR

The improvement of the data separator, or data recovery circuit, as it is called, is an important enhancement to the reliability of the VL1772-02. The operation of this part of the circuit, although critical to system reliability, is simple to understand. Figure 10 shows a train of read data pulses coming from a floppy drive. The clock and data pulses are both in this signal, combined in a simple encoding format. In each bit cell, the data separator chooses a time period within which pulses are recognized as data pulses. The better the resolution for defining this window for the data pulses, the greater the jitter in the signal can be before ones and zeros are incorrectly recognized. This incorrect recognition, and the resultant soft errors, are the basic limiting factor in floppy drive error rates. The VL1772-02, with a wider data window, has a lower chance of incorrect recognition, resulting in lower error rates. This effect will be particularly evident as the user's media degrades with use and jitter increases. This increased reliability of the VL1772-02 can result in fewer returns and greater user satisfaction.

FIGURE 10. WINDOWING READ DATA



STEP RATES

With a different selection of step rates than the 1770-00 (see table 9), the VL1772-02 allows the use of drives with minimum settle times up to 12 ms. At the same time, performance is enhanced to take advantage of floppy drives that require only 2 or 3 ms of delay. If a design is currently using head settle times of 6 or 12 ms (as most are), no modifications are required to use the VL1772-02 in the 1770-00 socket. If the current choice of r1 and r0 calls for 20 or 30 ms of delay, use of the VL1772-02 requires:

— the selection of drives that have head settle time under 12 ms, and modified software to allow correct r1, r0 choice, or

— implementation of head settle time in hardware, with an external interrupt.

Fortunately, almost all modern flexible disk drives have head settle times well under 12 ms, and current 1770 applications have taken this into account, using 6 or 12 ms as the head settle time. Where this change is required, it will mean less waiting for the drives to finish each seek. This will certainly produce higher user satisfaction with the system, as well as appreciably higher performance against most benchmarks.

TABLE 9. STEP RATE SELECTION: 1770-00 AND VL1772-02

Step Rate Select Bits		Step Rate (ms)	
r1	r0	1770-00	VL1772-02
0	0	6	6
0	1	12	12
1	0	20	2
1	1	30	3