TMS 2716-30 JL AND TMS 2716-45 JL
2048-WORD BY 8-BIT ERASABLE
PROGRAMMABLE READ-ONLY MEMORIES

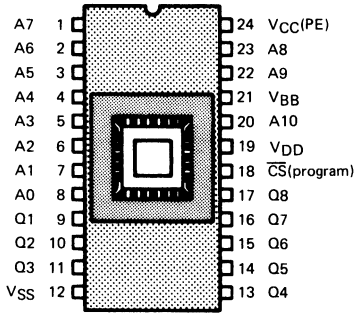
DECEMBER 1979—REVISED MAY 1982

- **2048 X 8 Organization**
- **All Inputs and Outputs Fully TTL Compatible**
- **Static Operation (No Clocks, No Refresh)**
- **Performance Ranges:**

	ACCESS TIME (MAX)	CYCLE TIME (MIN)
TMS 2716-30	300 ns	300 ns
TMS 2716-45	450 ns	450 ns

- **3-State Outputs for OR-Ties**
- **N-Channel Silicon-Gate Technology**
- **8-Bit Output for Use in Microprocessor-Based Systems**
- **Low Power . . . 315 mW (Typical)**

24-PIN CERPAK
DUAL-IN-LINE PACKAGE
(TOP VIEW)



5

description

The TMS 2716 is an ultra-violet light-erasable, electrically programmable read only memory. It has 16,384 bits organized as 2048 words of 8-bit length. The device is fabricated using N-channel silicon-gate technology for high-speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 circuits without the use of external pull-up resistors and each output can drive one Series 74 or 74LS TTL circuit without external resistors. The TMS 2716 guarantees 250 mV dc noise immunity in the low state. Data outputs are three-state for OR-tying multiple devices on a common bus. The TMS 2716 is plug-in compatible with the TMS 2708 and the TMS 27L08. Pin compatible mask programmed ROMs are available for large volume requirements.

This EPROM is designed for high-density fixed-memory applications where fast turn arounds and/or program changes are required. It is supplied in a 24-pin dual-in-line cerpak (JL suffix) package designed for insertion in mounting-hole rows on 600-mil (15.2 mm) centers. It is designed for operation from 0°C to 70°C.

operation (read mode)

address (A0-A10)

The address-valid interval determines the device cycle time. The 11-bit positive-logic address is decoded on-chip to select one of 2048 words of 8-bit length in the memory array. A0 is the least-significant bit and A10 most-significant bit of the word address.

chip select, program [$\overline{CS}$ (Program)]

When the chip select is low, all eight outputs are enabled and the eight-bit addressed word can be read. When the chip select is high, all eight outputs are in a high-impedance state.

program

In the program mode, the chip select feature does not function as pin 18 inputs only the program pulse. The program mode is selected by the V_{CC}(PE) pin. Either 0 V or +12 V on this pin will cause the TMS 2716 to assume program cycle.

data out (Q1-Q8)

The chip must be selected before the eight-bit output word can be read. Data will remain valid until the address is changed or the chip is deselected. When deselected, the three-state outputs are in a high-impedance state. The outputs will drive TTL circuits without external components.

operation (program mode)

erase

Before programming, the TMS 2716 is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (= UV intensity × exposure time) is fifteen watt-seconds per square centimeter. Thus, a typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in a minimum of 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state.

programming

Programming consists of successively depositing a small amount of charge to a selected memory cell that is to be changed from the erased high state to the low state. A low can be changed to a high only by erasure. Programming is normally accomplished on a PROM or EPROM Programmer, an example of which is TI's Universal PROM Programming Module in conjunction with the 990 prototyping system. Programming must be done at room temperature (25 °C) only.

to start programming (see program cycle timing diagram)

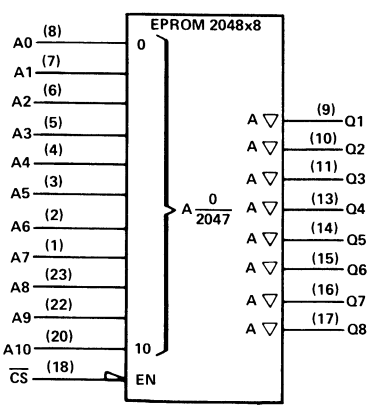
First bring the $V_{CC}(PE)$ pin to + 12 V or 0 V to disable the outputs and convert them to inputs. This pin is held high for the duration of the programming sequence. The first word to be programmed is addressed (it is customary to begin with the "0" address) and the data to be stored is placed on the Q1-Q8 program inputs. Then a + 26 V program pulse is applied to the program pin. After 0.1 to 1.0 milliseconds the program pin is brought back to 0 V. After at least one microsecond the word address is sequentially changed to the next location, the new data is set up and the program pulse is applied.

Programming continues in this manner until all words have been programmed. This constitutes one of N program loops. The entire sequence is then repeated N times with $N \times t_{W(PR)} \geq 100$ ms. Thus, if $t_{W(PR)} = 1$ ms; then N = 100, the minimum number of program loops required to program the EPROM.

to stop programming

After cycling through the N program loops, the last program pulse is brought to 0 V, then Program Enable $V_{CC}(PE)$ is brought back to ± 5 volts which takes the device out of the program mode. The data supplied by the programmer must be removed before the address is changed since the program inputs are now data outputs and a change of address could cause a voltage conflict on the output buffer. Q1-Q8 outputs are invalid up to 10 microseconds after the program enable pin is brought from $V_{IH(PE)}$ to $V_{IL(PE)}$.

logic symbol†



† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 289.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 to 15 V
Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 to 20 V
Supply voltage, V_{SS} (see Note 1) . . . . . −0.3 to 15 V
All input voltage (except program) (see Note 1) . . . . . −0.3 to 20 V
Program input (see Note 1) . . . . . −0.3 to 35 V
Output voltage (operating, with respect to V_{SS}) . . . . . −2 to 7 V
Operating free-air temperture range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 125°C

* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operating of the device at these or any other conditions beyond those indicated in the "Recommended Operting Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH} (except program and program enable)	2.4		$V_{CC}+1$	V
High-level program enable input voltage, $V_{IH(PE)}$	11.4	12	12.6	V
High-level program input voltage, $V_{IH(PR)}$	25	26	27	V
Low-level input voltage, V_{IL} (except program)	V_{SS}		0.65	V
Low-level program input voltage, $V_{IL(PR)}$ Note: $V_{IL(PR)}$ max ⩽ $V_{IH(PR)}$ − 25 V	V_{SS}		1	V
High-level program pulse input current (sink), $I_{IH(PR)}$			40	mA
Low-level program pulse input current (source), $I_{IL(PR)}$			3	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −100 μA	3.7			V
		I_{OH} = −1 mA	2.4			
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V		1	10	μA
I_O	Output current (leakage)	$\overline{CS}$ (Program) = 5 V, V_O = 0.4 V to 5.25 V		1	10	μA
I_{BB}	Supply current from V_{BB}	All inputs high,		10	20	mA
I_{CC}	Supply current from V_{CC}	$\overline{CS}$ (Program) = 5 V,		1	8	mA
I_{DD}	Supply current from V_{DD}	T_A = 0°C (worst case)		26	45	mA
I_{PE}	Supply current from PE on V_{CC} Pin	V_{PE} = V_{DD}		2	4	mA
$P_{D(AV)}$	Power Dissipation	T_A = 70°C			540	mW
		T_A = 0°C $\overline{CS}$ = 0V		315	595	
		T_A = 0°C $\overline{CS}$ = +5 V		375	720	

† All typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
C_i	Input capacitance [except CS (Program)]	4	6	pF
$C_{i(CS)}$	$\overline{CS}$ (Program) input capacitance	20	30	pF
C_o	Output capacitance	8	12	pF

† All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	TMS2716-30		TMS2716-45		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(ad)}$	Access time from address	C_L = 100 pF 1 Series 74 TTL Load $t_{f(CS)}$, $t_{f(ad)}$ = 20 ns See Figure 1		300		450	ns
$t_{a(CS)}$	Access time from $\overline{CS}$			120		120	ns
$t_{v(A)}$	Output data valid after address change		0		0		ns
t_{dis}	Output disable time†		0	120	0	120	ns
$t_{c(rd)}$	Read cycle time		300		450		ns

† Value calculated from 0.5 volt delta to measured output level.

T_A = 25°C program characteristics over recommended supply voltage range

PARAMETER		MIN	MAX	UNIT
$t_{w(PR)}$	Pulse width, program pulse	0.1	1	ms
t_T	Transition times (except program pulse)		20	ns
$t_{T(PR)}$	Transition times, program pulse	30	2000	ns
$t_{su(ad)}$	Address setup time	10		μs
$t_{su(da)}$	Data setup time	10		μs
$t_{su(PE)}$	Program enable setup time	10		μs
$t_{h(ad)}$	Address hold time	1000		ns
$t_{h(ad,da\ R)}$	Address hold time after program input data stopped	0		ns
$t_{h(da)}$	Data hold time	1000		ns
$t_{h(PE)}$	Program enable hold time	500		ns
$t_{CL,adX}$	Delay time, $\overline{CS}$ (Program) low to address change	0		ns

PARAMETER MEASUREMENT INFORMATION

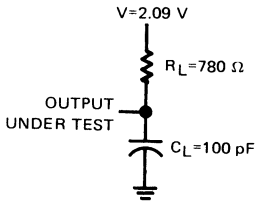
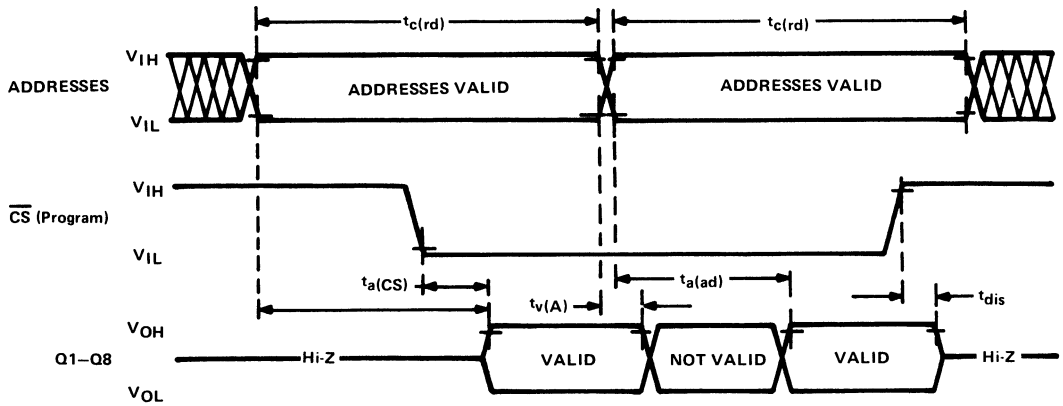


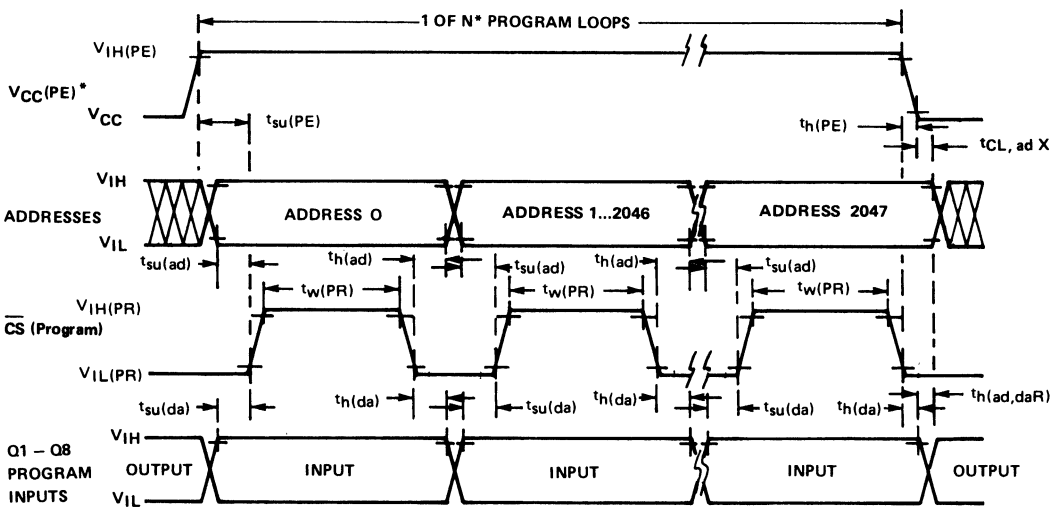
FIGURE 1 – TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing



5

program cycle timing



*V_{CC} (PE) is at 0 V or +12 V through N program loops where N $\geqslant$ 100 ms/tw (PR).

NOTE: Q1-Q8 outputs are invalid up to 10 μsec after programing (V_{CC} (PE) goes low).