PRELIMINARY

2817A
16K (2K x 8) ELECTRICALLY ERASABLE PROM

- 5 Volt Only Operation
- On-Chip Latches for Direct Microprocessor Interface
- Automatic Byte-Erase-before-Write
- Self Timed Byte Write
- Fast Read Access Time:
  - —2817A-1 200ns max
  - —2817A-2 200ns max
  - —2817A 250ns max
  - —2817A-3 350ns max
  - —2817A-4 450ns max
- Write Protect Circuit to Preserve Data on Power Up and Power Down
- 10,000 Erase/Write Cycles per Byte
- Reliable Intel HMOS*-E FLOTOX Cell Design Technology
- READY/$\overline{\text{BUSY}}$ Line for End-of-Write Signal
- 10 Year Data Retention For Each Write

The Intel 2817A is a 16,384 bit Electrically Erasable Programmable Read Only Memory. Like the Intel 2816A it has completely Non-Volatile Data Storage. In addition, it offers a high degree of integrated functionality which enables in-circuit byte writes to be performed with minimal hardware and software overhead. The Intel 2817A is a product of Intel's advanced E^2PROM technology and uses the powerful HMOS*-E process for reliable, non-volatile data storage.

*HMOS is a patented process of Intel Corporation.

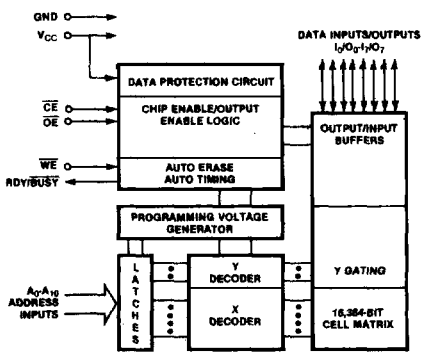

Figure 1. 2817A Functional Block Diagram

PIN NAMES

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	DATA OUTPUTS
I_0-I_7	DATA INPUTS
RDY/$\overline{BUSY}$	DEVICE READY/BUSY
N.C.	NO CONNECT
$\overline{WE}$	WRITE ENABLE

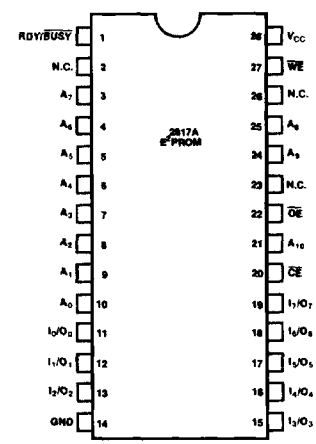

Figure 2. 2817A Pin Configuration

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The Intel 2817A incorporates all the interfacing hardware logic and the secondary voltage supply required to perform data writes. The device has complete self-timing which leaves the processor free to perform other tasks until the 2817A signals 'Ready'. With a transparent erase before write, the user benefits by saving an erase command which contributes to efficient usage of system processing time. On chip latching further enhances system performance.

The Intel 2817A's exceptionally fast read access time makes it compatible with high performance microprocessor applications. It uses Intel's proven 2-line control architecture which eliminates bus contention in a system environment. Combining these features with the 2817A's open drain 'Ready' signal makes the device an extremely powerful, yet simple to use, E^2 memory — available to the designer today.

The density, and level of integrated control, makes the Intel 2817A suitable for users requiring low hardware overhead, high system performance, minimal board space and design ease. Designing with, and using the 2817A, is extremely cost effective since all of the required programming voltage and interfacing hardware required for other E^2PROM devices has been eliminated. See Figures 1, 2, and 3 for the Intel 2817A's block diagram, pinout, and simple interface requirements.

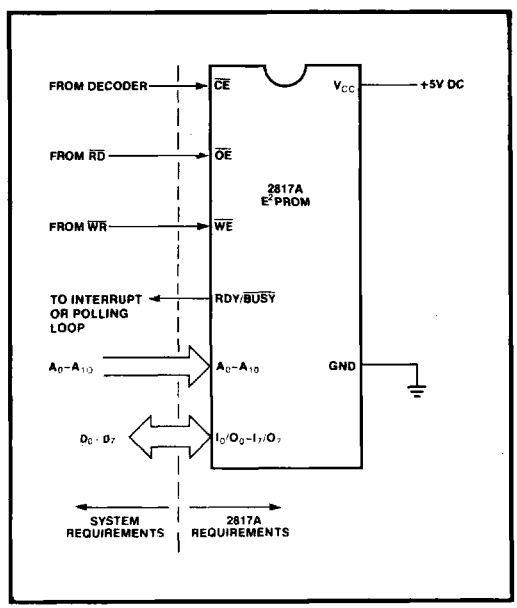


Figure 3. Simple 2817A Interface Requirements

DEVICE OPERATION

The Intel 2817A has 3 basic modes of user operation which are detailed in Table 1. All modes are designed to enhance the 2817A's functionality to the user and provide total Intel E^2PROM microprocessor compatibility.

Table 1. V_{CC} = +5V

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I_0/O_0-I_7/O_7	RDY/$\overline{BUSY}$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Hi-Z
Standby	V_{IH}	X	X	High Z	Hi-Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{OL}
Byte Erase	Automatic before each 'Write'				

NOTE: RDY/$\overline{BUSY}$ is an open-drain output with I_{OL} = 2.1 ma.

The Write Mode

The 2817A is programmed electrically in-circuit, yet it provides non-volatile storage without the constraint of ultraviolet erasure with EPROMs or of batteries with CMOS RAMs. Writing to non-volatile memory has never been easier as no external latching, erasing or timing are needed. When commanded to byte write, the 2817A automatically latches the address, data, and control signals, and starts the write. While the write operation is in progress, the RDY/$\overline{BUSY}$ output is low. The data bus is not used by the 2817A during the write operation, allowing the processor to perform other tasks.

After the write cycle is initiated with a $\overline{WE}$ strobe pulse, the 2817A completes the cycle off-line from the processor in two transparent steps. First, the existing data at the addressed location is automatically erased. At the beginning of this step the inputs are locked out, the data lines are brought to a high impedance state and the RDY/$\overline{BUSY}$ signal is lowered to V_{OL}. Second, the new data byte is written into the device. At the

end of this process, the 2817A raises its RDY/$\overline{BUSY}$ signal to V_{OH} to notify the processor that the write cycle is complete and that the device is ready for read or write access.

The write endurance is 10^4 cycles, that is, up to 10,000 write cycles can be reliably performed on each byte.

The Read Mode

One aspect of the 2817A's high performance is its fast read access time—typically less than 200 ns. Its read cycle is similar to that of EPROMs and static RAMs. The Intel 2817A can be selected using decoded system address lines to $\overline{CE}$ and then the device can be read, within the device selection time, using the processor's $\overline{RD}$ signal connected to $\overline{OE}$.

Read retention for data written into the 2817A is greater than 10 years.

The Standby Mode

The 2817A has a standby mode in which power consumption is reduced by 60%. This offers the user power supply cost benefits when designing a system with Intel 2817A's. This mode occurs when the device is deselected ($\overline{CE} = V_{IH}$). The data pins are put into the high impedance state regardless of the signals applied to $\overline{OE}$ and $\overline{WE}$ concurrent with the reading and writing of other devices.

On-Chip Data Protection on V_{CC} Power Up and Power Down

An erase/write of a byte in the 2817A is accomplished with input signals $\overline{CE}$, $\overline{WE} = V_{IL}$. During system (V_{CC}) power up and power down, this condition may be present as V_{CC} ramps up to or down from its steady state value of 5 volts. To prevent the possibility of an inadvertent byte write during this power transition period, an on-chip sensing circuit disables the internal programming circuit if V_{CC} falls below 4 volts (V_{LKO}).

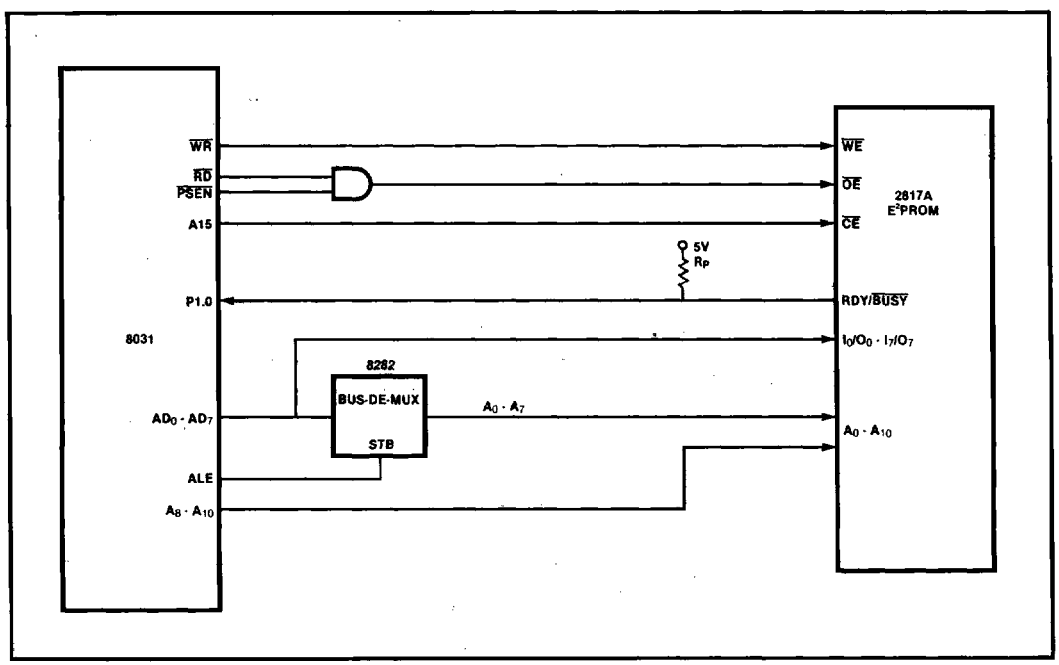


Figure 4. 2817A E^2PROM as Remotely-Alterable Non-Volatile Program Code Memory in an MCS® -51 System.

System Implementation

The 2817A is compatible with Intel MCS® -51 Microcomputer and the iAPX 86/88, 186/188, and 286 microprocessor families. The 2817A requires no interface circuitry. Figure 4 shows an example of the 2817A used as program storage memory in an 8031 single-chip microcomputer system. The 8031 program code is modified or upgraded remotely without having to remove the E^2PROM from the system.

The Intel 8282 8-bit latch shown in Figure 4 is used to de-multiplex addresses A0-A7. (The latch is typically required in any 8031 system.) The ANDing of signals $\overline{PSEN}$ and $\overline{RD}$ allows both program code and external data for the 8031 to be fetched/read from the 2817A E^2PROM. The 8031 determines when a given write cycle has been completed by reading port bit P1.0 which is connected to the 2817A's $\overline{RDY/BUSY}$ output.

Application Note AP-158 shows a complete schematic diagram of an 8088-based system design example. Included in AP-158 are various hardware design options for different applications and a number of 8088 code software routines for remote downloading applications,

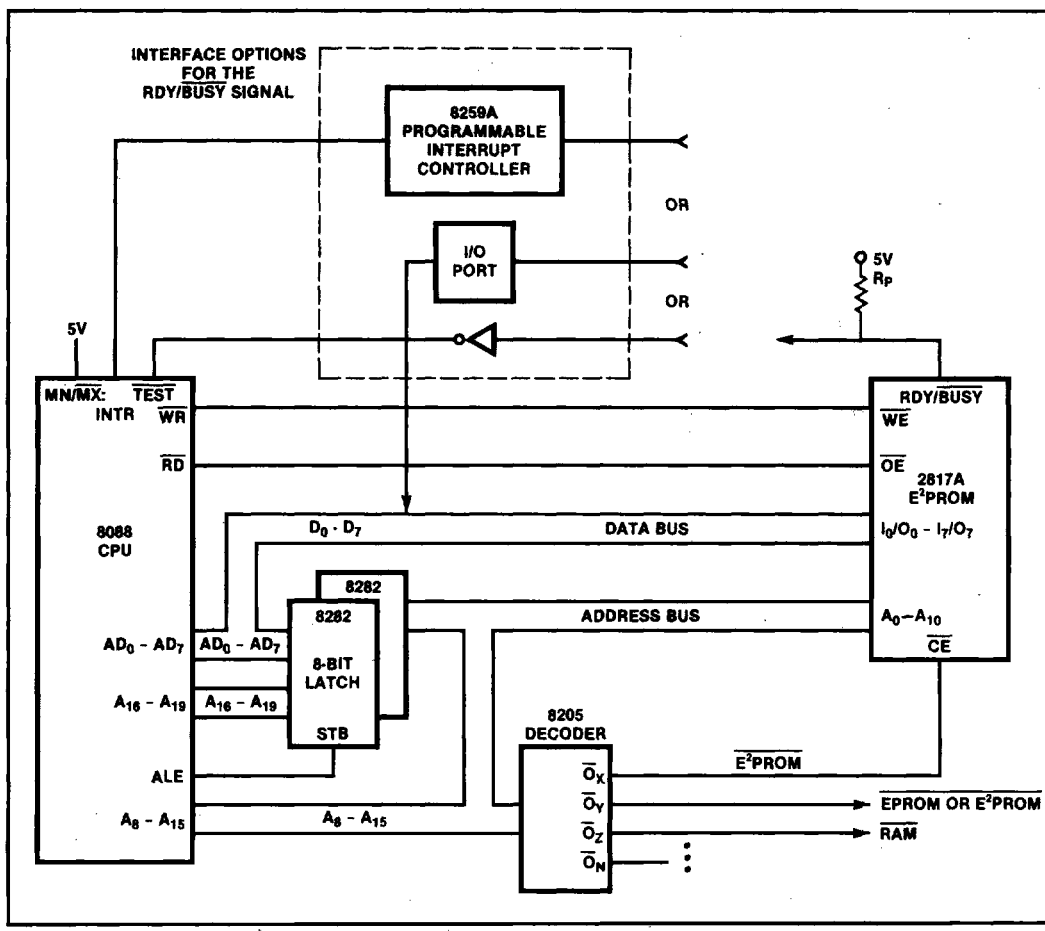


Figure 5. 2817A/8088 Interface Example

and for using the 8259A Programmable Interrupt Controller and the 8251A Programmable Communications Interface.

Interfacing to the Intel 8088 is similar to the 8031 interface. The difference lies in the use of the 8259A (Programmable Interrupt Controller). The Ready line can be connected to any of the interrupt request pins in order to interrupt the processor. (See Figure 5). Alternatively, it can be polled through an I/O port or connected through an inverter to $\overline{TEST}$ on the Intel 8088.

Using RDY/$\overline{BUSY}$

The RDY/$\overline{BUSY}$ pin is an open-drain output which allows two or more RDY/$\overline{BUSY}$ signals to be OR-tied together. To calculate the value of the pull-up resistor for the RDY/$\overline{BUSY}$ output, the following formula can be used:

$$R_P = \frac{4.6V}{2.1ma - I_{IL}}$$

where I_{IL} = the total V_{IL} input current of all devices connected to the RDY/$\overline{BUSY}$ line.

A typical pull-up resistor value for the RDY/$\overline{BUSY}$ output is 3.0K ohms, assuming that the input sink current (I_{IL}) of the input(s) being driven is less than 0.5 ma.

Applications

The Intel 2817A is ideal for non-volatile memory requirements in applications requiring storage of user defined functions, calibration constants, configuration parameters and accumulated totals. Soft key configuration in a character-oriented or graphics terminal is an example where user defined functions, such as protocol, color, screen attributes and character fonts can be keyed in by the user. Calibration constants can be stored in the 2817A with a smart interface for a robot's axis of movement. Movement constants, compensation algorithms and learned axis characteristics would be included. In programmable controllers and data loggers, configuration parameters for polling time, sequence and location, can be stored in the 2817A. Additional applications include accumulated totals for dollars, energy consumption, volume and even the logging of service performed on computer boards or systems for documentation purposes.

The Intel 2817A is cost effective for lower density E^2PROM applications and can therefore be used to provide a lower system cost to the user. The 2817A user will find that tangible cost savings per system include: board space and component reductions, reduced assembly costs, savings in inventory costs, handling costs and Quality Assurance. System designers will find the 2817A reduces design time by a sizeable factor due to the integration of timing, logic and latching.

The 2817A will also open up new applications in environments where flexible parameters/data storage could not be implemented before. Applications with board space constraints are ideal for the 2817A due to the on-chip integration of all functions required.

In Application Note AP-158 a comprehensive discussion of four major application areas for E^2PROMs is given:

1. Remote Firmware Downloading
2. System Re-Configuration (system parameter storage)
3. Maintenance Logging
4. Electronic Message Storage

Write Time Characteristics

The 2817A's internal write cycle contains an automatic erase feature. Furthermore, the 2817A automatically determines through its self-timer when a byte has been written and signals the completion via the Ready/$\overline{Busy}$ signal. The Ready/$\overline{Busy}$ signal is an open-drain output. The 2817A's internal cycle consists of an automatic 10 ms erase followed by a write. The total cycle is the time that Ready is held low by the device. The 2817A maximum specification is 20 ms for a combined Erase/Write cycle. The 2817A-1 is ideal for users desiring a faster erase/write cycle time. The total cycle time for this part is 10msec.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature..... −65°C to +100°C
All Input or Output Voltages with
Respect to Ground ..... +6V to −.3V

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND A.C. OPERATING CONDITIONS DURING READ AND WRITE

Temperature Range	0°C - 70°C
V_{CC} Power Supply	5V ± 5%

D.C. CHARACTERISTICS

Symbol	Parameter	Min.	Typ.(1)	Max.	Units	Test Conditions
I_{LI}	Input Leakage Current			10	μA	$V_{In} = V_{CC}$ Max.(2)
I_{LO}	Output Leakage Current			10	μA	$V_{Out} = V_{CC}$ Max.
I_{CCA}	V_{CC} Current (Active)		60	120	mA	$\overline{OE} = \overline{CE} = V_{IL}$
I_{CCS}	V_{CC} Current (Standby)			55	mA	$\overline{CE} = V_{IH}$, $V_{CC} = V_{CC}$ Max.
I_{CCW}	V_{CC} Current (Write)			150	mA	$\overline{WE}$ = ⊓⊔, $\overline{CE} = V_{IL}$
V_{IL} (D.C.)	Input Low Voltage (D.C.)	−0.1		.8	V	
V_{IL} (A.C.)	Input Low Voltage (A.C.)	−0.4			V	Time = 10ns
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			.45	V	$I_{OH} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400\mu A$
V_{LKO}	V_{CC} Level for Write Lockout	4.0		4.4	V	

NOTE:
1. This parameter only sampled and not 100% tested.
2. $I_{IL(max)}$ is less than 10μa when V_{IN} is less than 5.25V.

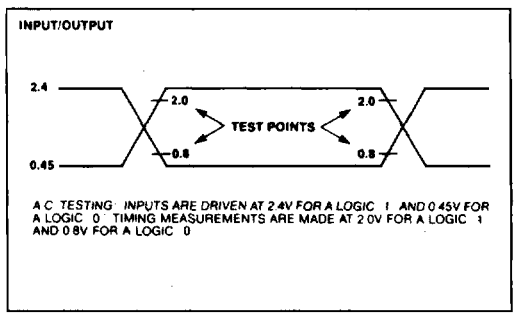
CAPACITANCE (T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Typ.(1)	Max.	Units	Test Conditions
C_{IN}	Input Capacitance	5	10	pF	V_{IN} = OV
C_{OUT}	Output Capacitance		10	pF	$\overline{OE} = \overline{CE} = V_{IH}$

A.C. TEST CONDITIONS

Output Load.....1 TTL gate + C_L = 100pF
Input Rise and Fall Times(10% to 90%).... 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level .... 0.8V and 2.0V
Output Timing Reference Level ... 0.8V and 2.0V

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. CHARACTERISTICS

READ

Symbol	Parameter	2817A-1 2817A-2 Limits			2817A Limits			2817A-3 Limits			2817A-4 Limits			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{ACC}	Address to Output delay.		150	200		200	250		300	350		400	450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay.		250	200		200	250		300	350		400	450	ns	
t_{OE}	$\overline{OE}$ to Output Delay.			75			100			120			150	ns	
t_{DF}(2)	$\overline{OE}$ High to Output not Driven	0		60	0		60	0		80	0		100	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0			0			0			0			ns	$\overline{CE}$, $\overline{OE} = V_{IL}$

NOTES:
1. This parameter only sampled and not 100% tested.
2. t_{DF} is measured from the point when $\overline{CE}$ or $\overline{OE}$ returns high (whichever occurs first) to the time when the outputs are no longer driven. This parameter is not 100% tested.

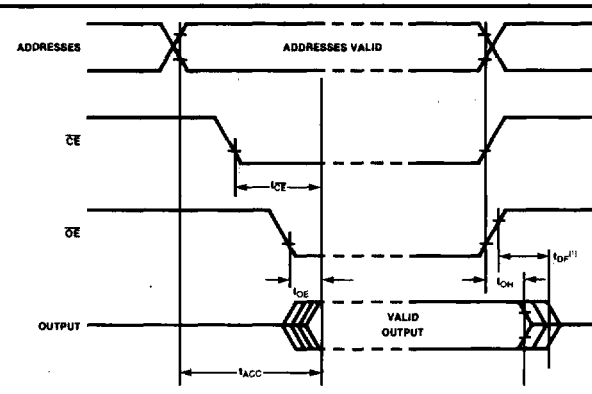
A.C. CHARACTERISTICS (Cont.)

WRITE

Symbol	Parameter	2817A-1			2817A-2			2817A 2817A-3			2817A-4			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{AS}	Address to write set-up time	20			20			20			60			ns
t_{CS}	$\overline{CE}$ to write set-up time	20			20			20			20			ns
t_{WP}	Write pulse width	100			100			100			200			ns
t_{AH}	Address hold time	50			50			50			110			ns
t_{DS}	Data set-up time	50			50			50			70			ns
t_{DH}	Data hold time	20			20			20			20			ns
t_{CH}	$\overline{CE}$ hold time	0			0			0			0			ns
t_{DB}	Time to Device Busy			120			120			120			120	ns
t_{WR}	Bytes Write Cycle Time		9	10		17	20		17	20		25	30	mS
	Number of Writes per byte	10^4			10^4			10^4			10^4			

WAVEFORMS

READ



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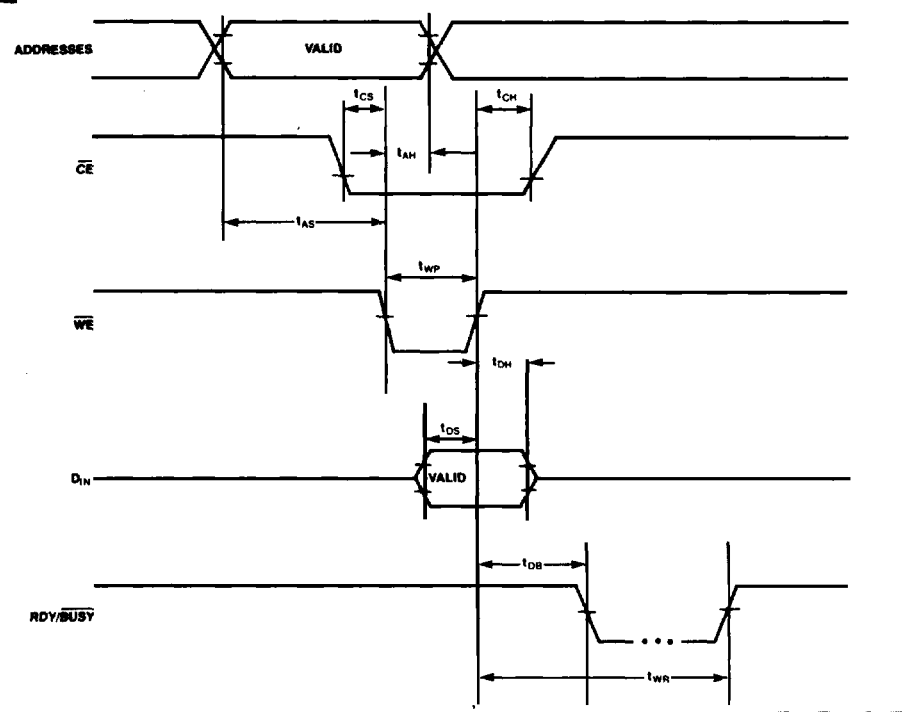
WRITE



AVAILABLE LITERATURE

The Intel E^2PROM family of devices, the 2816A and 2817A, is supported by many Application Notes. Topics covered range from Intel E^2PROM Technology and Reliability to Design considerations and Applications support for Designers implementing large arrays of E^2PROMs.

These notes and more are available in the Memory Components Handbook (Order No. 210830) or the Intel Literature Department, 3065 Bowers Ave., Santa Clara, CA 95051. To obtain this book contact your local Field Sales office. Your Field Applications Engineer is available to discuss all aspects of the Intel E^2 product line with you.